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A review of high-k dielectric materials for power electronic devices

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Abstract. Wide-bandgap semiconductors, represented by SiC and GaN, are central to the advancement of electronics technology. However, their gate dielectric engineering faces significant challenges. This paper employs a literature review and case studies to systematically examine the progress and future directions in high-k dielectric materials. The study traces their evolution from HfO_2 and Al_2O_3 to composite multilayers, elucidating the application mechanisms of key processes such as atomic layer deposition. Furthermore, the review demonstrates the applications of high-k dielectrics in enhancing SiC MOSFET gate oxide reliability and enabling low-voltage driving for flexible electronics. High-k dielectrics are critical in overcoming performance bottlenecks and advancing electric vehicles and smart grids. Future research should focus on interface defect control and on integration with ultra-wide bandgap semiconductors.

Keywords: high-k dielectric materials, power electronics, wide bandgap semiconductors, silicon carbide MOSFET, atomic layer deposition

1. Introduction

To align with the global energy transition trend and the Dual Carbon goals, efficient power conversion technologies are driving the development of wide bandgap semiconductor power devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN). Since SiC and GaN devices are designed to work under harsher conditions including higher voltage and temperature than traditional silicon-based devices, the performance of gate dielectric materials directly determines their upper limit of operational performance. Traditional Silicon Dioxide (SiO_2) is constrained by inherent limitations: low dielectric constant, numerous interface defects, and insufficient gate oxide reliability. These limitations are critical bottlenecks that impeds device performance enhancement. Research on high-k dielectric materials has successfully extended from logic devices to power electronics, becoming pivotal for overcoming these technical barriers.

Studies have explored the benefits of high-k materials. For example, Aluminum Oxide (Al_2O_3)/Hafnium Dioxide (HfO_2) multilayers markedly reduce interface state density in 4H-silicon carbide metal-oxide-semiconductor field-effect transistors (4H-SiC MOSFETs) [1]. Furthermore, Yu et al., confirms that nitrogen-doped HfO_2 films exhibit excellent high temperatures stability for high-power applications [2]. Nevertheless, gaps remain in the application research of high-k dielectric materials.

This paper systematically reviews the application of high-k dielectric materials in power electronic devices. It synthesizes current research to examine persistent challenges and future research directions. It aims to provide theoretical guidance for developing more efficient, reliable, and energy-saving power electronics.

2. Background and evolution of high-k dielectric materials

2.1. Fundamental properties and advantages

SiO_2, the traditional gate dielectric, has a dielectric constant (k) of approximately 3.9. In contrast, Hafnium Dioxide (HfO_2) and Zirconium Dioxide (ZrO_2) and other high-k dielectrics are significantly higher dielectric constants. Under identical gate capacitance conditions, high-k dielectrics enable increased physical thickness of the dielectric layer, which effectively suppressing gate leakage current caused by quantum tunneling effects [3]. Research has indicates that high-k dielectrics can reduce leakage current to less than one-tenth that of conventional SiO_2 gate dielectrics.

The advantages of high-k dielectric materials in power electronic devices are not limited to leakage current control. Next-generation wide-bandgap semiconductors require high-temperature and high-electric-field operating environments. High-k dielectrics simultaneously meet the high-barrier requirements of wide-bandgap materials while enhancing gate control capability through their high permittivity. Additionally, excellent interface characteristics and thermal stability constitute their key advantageous properties [4]. High-k dielectrics can also opitimize electric field distribution. Zhang et al. discovered that novel devices like Reverse-Conducting Insulated-Gate Bipolar Transistors (RC-IGBTs) can effectively optimize the trade-off between breakdown voltage and on-resistance through high-k back-gate structures [5].

2.2. Technology transfer from logic devices to power electronics

Initially, high-k dielectric materials were applied to microprocessor logic devices. As CMOS technology nodes scaled below 45nm, the physical limitations of SiO_2 gate dielectrics posed an insurmountable barrier. Leading manufacturers like Intel pioneered high-k metal gate technology to overcome this bottleneck, demonstrating its potential to enhance device performance and reliability. This laid the foundation for its tranfer into power electronics.

Howver, as high-k dielectrics transitioned from logic devices to power electronics, the research focus shifted from solely pursuing Equivalent Oxide Thickness (EOT). Reducing to comprehensively optimizing power device interface characteristics, high-temperature stability, and long-term reliability is the other change. Research on high-k gate dielectrics for 4H-SiC-based power devices has evolved from single-material systems to multifunctional composite structures. These structures aim to synergistically enhance thermal stability, interface quality, and relectric field stress resistance while maintaining high dielectric constants [6].

3. Innovative developments in high-k dielectric materials

3.1. Material system transformation

3.1.1. Single oxide systems

Single-oxide systems were the focus of early research, including HfO_2, Al_2O_3, and ZrO_2. HfO_2 and ZrO_2 both have a dielectric constant of around 25, while Al_2O_3 has a relatively lower dielectric constant of around 9. Although HfO_2 has the highest dielectric constant, its bandgap offset with SiC is approximately 1.5 eV, which easily induces gate leakage. Al_2O_3 offers the widest bandgap has the widest bandgap, at approximately 8.8 eV,

along with excellent interfacial properties, though its dielectric constant is a clear drawback. ZrO_2, meanwhile, faces challenges related to crystallinity and interfacial stability [7].

3.1.2. Nanolayered and composite structures

To overcome the limitations of single-oxide layers, researchers have further developed nanolayered and composite structures. The HfO_2/ZrO_2 nanolayer structure, with individual layers only 2–3 nm thick: it maintains a high dielectric constants, and suppresses the phase transition tendencies of each material interfacial effects. Experiments results demonstrated that this structure can enhance the thermal stability of the film to more than 800°C [8]. The HfO_2/Al_2O_3 layered structure applied in 4H-SiC MOSFETs is more representative; when using as a gate dielectric, nanolayer structure relies on Al_2O_3 to achieve excellent interface passivation, and HfO_2 to provide high capacitance density. This structure reduces the device interface state density to below 2×10^{11} $cm^{-2}eV^{-1}$, while maintaining outstanding gate control capability.

3.1.3. Elemental doping

Elemental doping is a key process for optimizing the performance of high-k dielectric. Doping with elements such as La, Si, and N is an effective strategy for tuning the properties of HfO_2 film [9]. 5–10% La doping stabilizes the cubic phase of HfO_2, increases the dielectric constant to 30–35, and raises the oxygen vacancy formation energy by approximately 0.5 eV. Meanwhile, a 5% Si-doped $HfSiO_4$ structure raises the crystallization temperature of HfO_2 to over 900°C, enhancing the film's thermal stability. Approximately 3% N doping passivates defects at the HfO_2/SiC interface and suppresses grain boundary diffusion, reducing the fixed charge density at the interface from 10^{12} cm^{-2} to the 10^{11} cm^{-2} range [9].

3.2. Preparation and process optimization

3.2.1. Atomic Layer Deposition (ALD) technology

Atomic Layer Deposition (ALD) technology has become the preferred technique for fabricating high-k due to its excellent film uniformity, precise thickness control, and 3D conformality.

Plasma-Enhanced ALD (PEALD) enables deposition of high-quality HfO_2 films at relatively low temperatures of 250–300°C, with thickness uniformity below 1% and batch-to-batch variation less than 2% [10]. This technology also enables uniform coating on three-dimensional structures, preventing localized gate weak points and facilitating the construction of nanostacked layers and precise doping. It provides a crucial pathway for the controlled fabrication of high-performance high-k dielectrics.

3.2.2. Post-deposition annealing process

Post-Deposition Annealing (PDA) is a critical post-processing step for optimizing high-k dielectric performance. Under appropriate conditions, it significantly enhances electrical properties and reliability. Annealing at 800–900°C in an N_2O atmosphere passivates defects at the HfO_2/SiC interface, reducing the interface state density from the 10^{12} $cm^{-2}eV^{-1}$ range to below 10^{11} $cm^{-2}eV^{-1}$.

Compared with conventional furnace annealing, RTA offers more precise temperature control and shorter processing times. This prevents interfacial degradation caused by prolonged high-temperature exposure [11].

High-k dielectric materials, through synergistic optimization of material systems and fabrication processes, sucessfully overcome its performance limitatiosn. With elemental doping for property tuning, material systems evolve from single oxides to composite structures. Fabrication and post-processing techniques, such as ALD for ultra-thin uniform films and PDA for optimizing film crystallinity and interface state density are simultaneously upgraded. The realization of high-performance high-k dielectrics stems from the deep integration of material innovation and process optimization.

4. Typical applications

4.1. Interface optimization in SiC MOSFETs

The SiC/SiO_2 interface has a high density of interface states. It is formed by native thermal oxidation and inhibits carrier mobility in the channel. Wang and other scholars found that these interfaces will cause Coulomb scattering. Sometimes, it even reduces carrier mobility and induces significant threshold-voltage instability under high-temperature, high-voltage operating conditions. Therefore, it is regarded as a threat to device long-term reliability [12]. The real reason is the presence of numerous unsaturated silicon-carbon bonds and carbon clusters at the SiC/SiO_2 interface. To solve this problem, using Al_2O_3 or HfO_2/Al_2O_3 multilayer structures is an effective method. Al_2O_3 exhibits lower interface-trap formation and can reduce the interface-state density to below 2×10^{11} $cm^{-2}eV^{-1}$, while maintaining excellent gate control capability [13]. This interface optimization increases channel carrier mobility by nearly three times. Correspondingly, the on-resistance of SiC MOSFETs incorporated with high-k dielectrics decreases [14]. These improvements mitigate temperature instability, enabling SiC MOSFETs to maintain outstanding switching characteristics at high temperatures [15].

4.2. Low-voltage operation of flexible power devices

Flexible power devices not only require low-voltage operation but also mechanical flexibility and safety. Traditional dielectric materials failed to balance high capacitance density with flexibility. High capacitance density is precisely the core prerequisite for low-voltage operation of devices. When capacitance is insufficient, the energy storage demand needs to be made up by increasing the voltage. Then, it often results in operating voltages exceeding 10V, increasing power consumption, shortening battery life, and introducing safety risks.

High-k polymer composites have sophisticated molecular design and nanostructure engineering. The material can synergize high dielectric constants with excellent mechanical flexibility. High-k dielectrics can increase capacitance per unit area by enhancing the dielectric constant. This enables device operation below 5 V while maintaining the required physical thickness.

Research has proven this potential. Guo et al. developed a hybrid dielectric film comprising a Zinc Chloride ($ZnCl_2$) polymer electrolyte. As a typical high-dielectric-constant polymer composite, this film has been successfully applied in Organic Field-Effect Transistor (OFET) memory due to its optimized dielectric properties [16]. The results show that the film can achieve a wide storage window of 0.548V at a low voltage of -1.5V. Its low-voltage characteristic is directly related to the high capacitance density brought about by the high dielectric constant, providing a low-power consumption solution for flexible storage devices in the field of image processing [16].

What's more, an ultra-flexible energy-harvesting-storage-integrated system was developed by Xiao and his team. It successfully combines ultra-flexible Organic Photovoltaic (OPV) modules with ultra-thin zinc-ion batteries [17]. As a complementary power supply solution for flexible power devices, it works synergistically with low-voltage devices supported by high-dielectric-constant materials, further improving the energy supply system of flexible electronic systems. At present, High-k polymer materials provide a low-power solution for flexible storage devices in the field of image processing.

5. Discussion

5.1. Challenges

Despite promising prospects for high-k dielectric materials in power electronics, large-scale implementation faces multiple core technical challenges. The problems mainly focus on two aspects: interface defect control and gate leakage suppression. In addition, the long-term reliability of such materials still needs to be tested.

For interface defect control, the defect density at high-dielectric-constant/wide-bandgap semiconductor interfaces remains more than an order of magnitude higher than that of traditional dielectric material systems. Related studies show that even under optimized fabrication conditions, the interface trap density of high-dielectric-constant materials remains as high as 5×10^{11} $cm^{-2}\cdot eV^{-1}$, far exceeding the upper limit of traditional systems [18]. Such high-density interface traps will severely limit the channel carrier mobility and reduce the operational reliability of devices during flexible deformation and repeated start-stop processes, becoming the core obstacle hindering the application of high dielectric constant materials in flexible power devices [18].

Gate leakage is another critical challenge. Infineon Technologies proved that leakage current in high-k gate dielectrics increases by approximately two orders of magnitude at 150°C compared to room temperature [19]. Because some applications of flexible power devices often involve temperature fluctuations, this characteristic directly limits their use in high-temperature flexible applications. Furthermore, long-term reliability issues are pronounced in power electronics applications, where charge trapping/detrapping under electric-field stress directly contributes to threshold-voltage instability.

5.2. Future directions

Although there are still technical challenges to the large-scale application of these kinds of materials, the exploration of their application by emerging strategic industries such as new energy vehicles and renewable energy is still in its early stages. In the electric vehicle drive systems of many companies, Silicon Carbide (SiC) MOSFETs with high-dielectric-constant gate dielectrics have begun to be used. Related research shows that this device can effectively improve the energy conversion efficiency of inverters, thereby extending the driving range of electric vehicles by 5-8%, or reducing the battery capacity configuration requirements by about 10% [20].

At the same time, high dielectric constant materials can also enhance the operational reliability of power devices, extend the service life of systems, and thus reduce the overall maintenance cost.

High-k dielectric research is increasingly interdisciplinary. New material exploration is shifting toward multi-component compounds and customized materials. Two-dimensional layered materials such as $GaPS_4$ and hexagonal Boron Nitride (h-BN) are promising candidates. These materials have inherent van der Waals interfaces and atomically precise interface control via selective ALD. These features make them ideal for optimizing the properties of the high-k/semiconductor interface [21]. Another innovative approach combines multiscale simulation with artificial intelligence. Molecular dynamics modeling enables the atomic-level elucidation of structure-property relationships in high-k dielectrics.

6. Conclusion

This paper systematically reviews the typical applications and underlying mechanisms of high-k dielectric materials in power electronic devices. Research confirms that high-k dielectrics play a pivotal role in enhancing power electronics, especially for flexible devices and wide-bandgap semiconductor systems like SiC MOSFETs. They serve as a key driver propelling power electronics technology toward high efficiency,

high frequency, and high integration. Furthermore, challenges persist, including high interface defects, elevated gate leakage at high temperatures, and threshold voltage instability. The paper also points out that future directions involve interdisciplinary research, such as multi-component materials, 2D layered materials ($GaPS_4$, h-BN), and AI-integrated simulation to optimize performance.

However, this study has certain limitations. It relies mostly on secondary data, lacking first-hand experimental validation of process parameters. It also overlooks industrial pain points like high ALD possess costs formass production consistency. Future research should incorporate detailed process experiments and device simulations for more in-depth quantitative validation.

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