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Semiconductor nanostructures: rational design, controllable fabrication, interface regulation, and multi-field applications

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Abstract. In the post-Moore's Law era, traditional bulk semiconductor devices are approaching fundamental physical limits, making it difficult to meet the demands for high integration, miniaturization and multifunctionality of next-generation electronics. Semiconductor nanostructures, with unique quantum size, surface, and confinement effects, have become the core means of breaking through these bottlenecks. This review systematically summarizes the latest research progress in the rational design, controllable fabrication and multi-field applications of semiconductor nanostructures, and focuses on the technical characteristics and pros and cons of precise preparation of single-unit nanostructures, directional construction of composite heterostructures, preparation of doped/modified nanostructures and epitaxial growth of low-dimensional single-crystal nanostructures. It elaborates on the performance optimization mechanisms and practical application values of nanostructures in optoelectronic, chemical/gas sensing and energy conversion devices, and deeply analyzes the core challenges in wafer-scale fabrication integration, device performance reliability and interface compatibility. Corresponding targeted interface regulation strategies are further proposed and discussed, including δ-doping engineering, van der Waals epitaxy and low-temperature etching technology. This review clarifies the key technical paths for the performance regulation of nanostructured semiconductor devices and provides a comprehensive theoretical and technical reference for the industrial development of high-performance nanostructured semiconductor devices in the post-Moore era.

Keywords: Semiconductor nanostructures, Controllable fabrication, Interface regulation, Optoelectronic devices, Sensing and energy conversion devices

1. Introduction

Semiconductor devices are the cornerstone of modern microelectronics, optoelectronics, and energy conversion systems. Their performance evolution has long been driven by dimensional downscaling and structural innovation. In the post-Moore's Law era, however, continued miniaturization of traditional bulk semiconductors faces fundamental physical constraints such as short-channel effects and quantum tunneling, making it increasingly difficult to satisfy the growing demands for high efficiency, miniaturization, and multifunctionality in advanced electronic systems. Semiconductor nanostructures have emerged as a critical research frontier for overcoming these bottlenecks, leveraging unique quantum size, surface, and confinement effects that enable precise modulation of their electronic, optical, and catalytic properties.

This review systematically surveys research achievements over the past decade, primarily drawing on high-quality journals articles and landmark studies published since 2015. It comprehensively examines core fabrication techniques, representative device applications, and key challenges restricting their industrialization, with a particular focus on interface regulation strategies. This study aims to clarify the development law of nanostructured semiconductor devices and points out the key research directions for their practical application.The research on semiconductor nanostructures is of great significance in promoting the innovation of semiconductor device technology, breaking the technical monopoly of traditional silicon-based semiconductors, and accelerating the development of next-generation microelectronics and optoelectronics industries.

2. Nanostructure design, construction and controllable preparation technology

Nanostructure engineering serves as the foundational cornerstone for high-performance semiconductor devices, with advanced controllable preparation enabling atomic-level tailoring of nanoscale material morphology, composition, and interfacial properties [1].

Driven by demands for device miniaturization, multifunctionalization, and reliability, wafer-scale fabrication and heterogeneous integration of nanostructures have become the core pursuit of current research, providing indispensable technical support for next-generation semiconductor device integration and performance optimization. Meanwhile, the characteristics and limitations of different preparation technologies make route selection crucial for nanostructure performance and applications [2, 3].

2.1. Precise preparation of single-unit nanostructures

The precise preparation of single-unit nanostructures aims to achieve accurate control over size, morphology, and crystallinity with high reproducibility, relying on advanced micro/nano-fabrication technologies. Chemical vapor deposition (CVD), as the mainstream technique, enables controllable growth of 1D nanostructures (e.g., carbon nanotubes, perovskite nanowires) with high crystallinity and strong tunability, although it suffers from long preparation cycles and limited yield [4]. Plasma/laser fabrication offers ultrahigh precision and uniformity for high-aspect-ratio nanochannel arrays, supporting vertical device integration, but entails high equipment cost and complex process control [5]. Solution-based and low-temperature atmospheric plasma methods feature low cost, simple operation and large-area scalability, suitable for mass production of metal oxide and organic semiconductor nanostructures, despite relatively low structural precision [6, 7]. Microwave synthesis provides rapid, low-energy preparation of functional nanostructures, yet is restricted by limited production scale [8].

2.2. Directional construction of composite heterostructures

Directional construction of composite heterostructures enables multifunctional integration by regulating interface contact, lattice matching and charge transfer. CVD-fabricated core-shell van der Waals heterostructures exhibit tight interfacial bonding and efficient charge separation, suitable for high-quality heterostructure growth [4]. In-situ growth forms robust, defect-free interfaces, significantly boosting electrocatalytic performance [9]. Hydrothermal synthesis enables hierarchical heterostructures with abundant oxygen vacancies under mild conditions, which is favorable for electrochemical applications [10]. Multicomponent heterostructures prepared by deposition and p-n/S-scheme heterojunction design optimize carrier separation and transport, enhancing sensing and photocatalytic performance [11-13].

2.3. Preparation of doped and surface-modified nanostructures

Doping and surface modification provide effective strategies for tuning the electronic structure, defect states, and interfacial properties of semiconductor nanostructures. These strategies can be broadly classified into carrier regulation, optical property modulation, and interface engineering.

Carrier regulation is commonly achieved through metallic and non-metallic doping, which adjusts carrier concentration and defect density, thereby enhancing the gas sensing and optoelectronic performance of semiconductor nanostructures [6, 14].

Optical property modulation is mainly realized via rare-earth ion doping, which enables tunable photoluminescence and extends applications in multifunctional optoelectronic devices [15].

Interface engineering relies on δ-doping engineering and noble metal surface modification, which precisely regulate spin-orbit coupling and interfacial charge transfer, thus optimizing the performance of spintronic and photodetection devices [16, 17].

2.4. Epitaxial growth of low-dimensional single-crystal nanostructures

Wafer-scale epitaxial growth of low-dimensional single-crystal nanostructures is the key to industrialization, requiring large-area uniformity, high crystallinity, and substrate compatibility. Low-cost wafer-scale Au(111) single crystals provide ideal epitaxial substrates for high-quality 2D layered materials, ensuring uniform large-area films at low cost [18]. Microwave plasma chemical vapor deposition (MPCVD) enables homoepitaxial growth of single-crystal diamond nanostructures with excellent electronic and optical properties, supporting applications in high-power devices and nano-electromechanical systems. This method features a high growth rate but relatively high equipment cost [19]. Wafer-scale epitaxy of atomically thin single-crystal insulators delivers high-performance substrates for 2D field-effect transistors, resolving interface mismatch in heterogeneous integration [3]. 2D material-assisted van der Waals (vdW) epitaxy effectively eliminates lattice mismatch, improves epitaxial film quality, and extends optoelectronic applications, making it highly suitable for heterogeneous nanostructure growth [20].

3. Nanostructures in semiconductor optoelectronic device

Nanostructure engineering brings revolutionary breakthroughs for semiconductor optoelectronic devices. The tailorable optical, electronic, and interfacial properties of low-dimensional nanostructures enable precise modulation of light-matter interaction, carrier transport dynamics, and spin-photon coupling [11]. Rational nanostructure and heterointerface design breaks the bottlenecks of conventional optoelectronic devices, driving the development of high-efficiency, miniaturized, and multifunctional systems integrating light emission, photodetection, and spin manipulation [15]. Continuous innovation in nanostructure design and fabrication has significantly improved luminous efficiency, detection sensitivity, response speed, and spin polarization, among which interface and morphology optimization are the core means of performance enhancement [21].

3.1. Light-emitting devices

Nanostructure engineering provides an effective pathway for advancing the performance of semiconductor light-emitting devices (LEDs), particularly in terms of luminous efficiency, operational stability, and emission characteristics.

Perovskite nanostructures, benefiting from strong quantum confinement and high photoluminescence quantum yield, have emerged as promising candidates for high-efficiency LEDs. For example, vertically aligned perovskite nanowire arrays with high crystallinity and orientation can effectively suppress interfacial non-radiative recombination, thereby enhancing luminous efficiency [5]. Heterostructure engineering further improves device performance by optimizing charge injection and transport.

Core-shell nanostructures and van der Waals heterostructures enable efficient carrier separation and reduced recombination losses due to improved band alignment and strong interfacial coupling, resulting in enhanced emission stability. In addition, nanostructure design plays a crucial role in improving light extraction efficiency. For instance, scattering nanostructures introduced in deep-ultraviolet LEDs significantly enhance photon extraction, but high fabrication costs still hinder large-scale application [22].

3.2. Photodetection and infrared devices

Nanostructured materials serve as core building blocks for high-performance photodetection and infrared devices, governing detection sensitivity, response speed, bandwidth, and flexibility. Unique optical absorption, charge separation, and transport properties enable broadband, high-sensitivity, and fast-response photodetection [17]. Two-dimensional Ruddlesden–Popper perovskite $Cs_2PbI_2Cl_2$ nanostructures realize self-powered visible-blind ultraviolet photodetectors, with tunable bandgap and high crystallinity enabling selective UV absorption and efficient photoelectric conversion [23]. Ag-doped ZnO nanostructures are employed in flexible MSM UV photodetectors, maintaining stable photoresponse under mechanical deformation for wearable optoelectronic applications [6].

Ternary $TiO_2/MoS_2/ZnO$ hetero-nanostructures extend detection bandwidth and suppress charge recombination via heterointerface engineering, improving photodetection efficiency [11]. High-performance uncooled PbSe/CdSe nanostructured photodetectors with tunable cutoff wavelength satisfy the requirements of miniaturized mid-infrared sensing systems [24]. Current challenges include limited sensitivity of mid-infrared devices, environmental instability of perovskite photodetectors, and high cost of uncooled infrared detectors.

3.3. Spintronic optoelectronic devices

Nanostructure engineering has enabled precise manipulation of spin-orbit phenomena, providing a foundation for the development of semiconductor spintronic optoelectronic devices that integrate spin and photon functionalities.

Control of spin-orbit-coupling (SOC) is central to these devices. Nanostructures with tailored geometries and eletronic properties can modulate SOC strength, enabling efficient spin filtering and spin-polarized carrier transport [25]. For example, Rashba and Dresselhaus SOC-based nanostructures allow selective transmission of spin-polarized carriers, which is essential for spintronic device operation [16]. Doping engineering further enhances spintronic performance by enabling precise regulation of spin polarization and relaxation dynamics. Techniques such as δ-doping provide localized control of electronic states, while rare-earth or transition-metal doping introduce coupled optical and magnetic functionalities, facilitating multifunctional device applications.

In addition, advanced nanostructures such as semiconductor quantum wells ennable nonreciprocal photonic behavior, allowing directional propagation of spin-dependent light and open possibilities for optical information processing and quantum communication.

Despite significant progress, challenges remain, including low spin polarization efficiency, short spin relaxation times, and difficulties in device integration, which limit practical applications.

4. Nanostructures in semiconductor sensing and energy devices

Nanostructure engineering serves as a core driver for advancing high-performance semiconductor sensing and energy devices. The exceptional surface activity, charge transport kinetics, and energy conversion characteristics of low-dimensional nanostructures enable precise modulation of device sensitivity, selectivity, and efficiency [11, 14]. Rational design of nanostructure morphology, composition, and heterointerfaces effectively breaks the performance bottlenecks of conventional devices, laying a foundation for miniaturized, integrated, and sustainable sensing and energy systems.

4.1. Chemical/gas sensor devices

Nanostructured semiconductor materials are widely used in chemical and gas sensors due to their enhanced surface reactivity and tunable electronic properties. The key performance metrics include sensitivity, selectivity, response/recovery speed, and detection limit.

Defect engineering, particularly through the introduction of oxygen vacancies, is an effective strategy to enhance gas sensing performance.For instance, doped ZnO nanostructures exhibit increased surface adsorption activity and improved charge transfer efficiency, thereby leading to enhanced sensitivity toward target gases such as NO_2.

Heterstructure design further improve sensing performance by modulating carrier transport. p-n heterojunctions enable efficient separation and migration of charge carriers, thereby enhancing both sensitivity and selectivity under varying environmental conditions. Surface modification techniques, including plasma treatment and atomic layer deposition, optimize surface adsorption properties and interfancial wettability, enabling reliable sensing performance in complex environments.

At present, the main challenges of nanostructured chemical/gas sensors are poor selectivity in complex environments, high detection limit of trace gases, and long-term instability of sensors.

4.2. Photovoltaic and solar energy conversion devices

Nanostructure design is essential for improving the performance of photovoltaic and solar energy conversion devices, for which the key indicators include photoelectric conversion efficiency, stability, and cost-effectiveness.

Light absorption can be significantly enhanced through nanostructure engineering. For example, plasmonic Al nanoparticles modified InP nanostructures achieve efficient light trapping in hexagonal InP nanostructured solar cells, significantly improving the photoelectric conversion efficiency by enhancing light absorption and charge separation, and the plasmonic effect of metal nanoparticles is an effective way to enhance the light absorption of photovoltaic devices [26]. Heterostructure engineering plays a central role in promoting efficient charge separation and transport. Perovskite-based nanostructures and their heterostructures enable multi-channel carrier transport and suppress charge recombination, effectively improving the photovoltaic performance [4].

Nanostructure engineering, interface optimization, and prelithiation effectively alleviate volume expansion in silicon-based nanostructures and improve the photoelectric conversion efficiency of silicon photovoltaic devices, thus realizing the integration of solar conversion and energy storage [27]. Rational interface and heterostructure design also enhance the efficiency of photoelectrochemical water splitting in nanostructured solar cells [28]. Post-treatment and interface cocatalyst engineering further optimize the photocatalytic hydrogen evolution performance of TiO2-based nanostructures, thereby facilitating the development of high-efficiency solar energy conversion devices [29].However, challenges such as poor long-term stability of perovskite materials and high fabrication costs of high-efficiency devices still hinder large-scale commercialization.

4.3. Novel energy harvesting devices

Novel energy harvesting devices rely on nanostructure engineering to achieve efficient energy collection, conversion, and storage, for which hierarchical heterostructures and interface optimization are the dominant design strategies [9].

For electrochemical energy storage, urchin-like molybdenum-manganese oxide heterostructures with abundant oxygen vacancies exhibit accelerated ion diffusion and enhanced redox activity, serving as high-performance cathodes for quasi-solid-state zinc-ion batteries [10]. MXene quantum dot modified AlCoS nanocube composites deliver ultrahigh energy density in asymmetric supercapacitors, benefiting from multi-component interface synergy and hierarchical nanostructure design [30].

In electrocatalytic energy conversion, nanostructured Ni_2P-Ni_5P_4/NF heterostructures enable efficient hydrogen evolution via water electrolysis, providing a feasible route for clean hydrogen production [9].

For ambient and waste heat energy harvesting, triboelectric nanogenerators (TENGs) and hydrovoltaic devices based on nanostructured materials achieve efficient mechanical and biochemical energy collection from human motion and sweat [31, 32].Interface engineering of polyethyleneimine/carbon nanotube composites significantly boosts thermoelectric performance, thereby enabling effective waste heat recovery for wearable and distributed energy systems [33].

Despite these advances, low energy conversion efficiency, limited energy density, and insufficient mechanical stability remain major challenges for practical applications in wearable electronics and clean energy systems.

5. Core challenges and interface regulation strategies

Despite remarkable progress in nanostructured semiconductor devices, their industrialization and large-scale application are still hindered by critical challenges in fabrication, integration, performance, and reliability [3]. Interface regulation has become the key to addressing these issues, as it can effectively improve interfacial compatibility, reduce defect density, and optimize charge transport [2, 13].

5.1. Core challenges

Wafer-scale uniform preparation and heterogeneous integration represent the primary fabrication bottleneck. Conventional growth methods suffer from low yield, poor uniformity, and high cost, while lattice mismatch and thermal expansion differences lead to interface defects, dislocations, and poor film quality [3, 18]. The integration process easily causes structural distortion and interface damage, degrading carrier transport and device performance [4, 5]. Meanwhile, the large-scale, low-cost fabrication of wide-bandgap and single-crystal nanostructures remains difficult [8, 19].

Device performance and reliability are mainly limited by interface states, high contact resistance, Fermi-level pinning, and poor interfacial contact [6]. Long-term operation induces interface degradation, ion migration, and surface oxidation, all of which severely reduce stability and service life, especially for perovskite and flexible devices [23]. Short-channel effects and interface scattering further degrade electrical performance and restrict practical applications [34].

5.2. Interface regulation strategies

Surface modification and defect passivation can optimize wettability, reduce trap states, and enhance interfacial bonding. Plasma treatment, atomic layer deposition, organic/inorganic passivation, and noble metal decoration effectively suppress defects, ion migration, and oxidation, thereby improving stability and reactivity [17, 35].

Doping engineering and energy band regulation precisely tune carrier concentration, defect density, and spin–orbit coupling. δ-doping, nonmetallic doping, metal doping, and rare-earth doping optimize band alignment, carrier transport, and spin-related properties [6, 14-16].

Epitaxial growth and interface matching optimization, especially van der Waals epitaxy and wafer-scale single-crystal epitaxy, alleviate lattice mismatch and enable high-quality heterogeneous integration [3, 20]. Atomic-level precise construction eliminates interfacial mismatch and realizes seamless connection between heterogeneous layers [1].

Low-temperature and high-precision etching purifies interfaces, removes contaminants, and reduces trap density without introducing damage, thereby improving carrier mobility and device uniformity [5]. Heterojunction design including p–n junctions, core–shell structures, and S-scheme heterostructures promotes efficient charge separation and suppresses recombination. Interface engineering and cocatalyst modification enhance charge transfer and photocatalytic performance [4, 12, 13, 29].

6. Conclusion

This review systematically summarizes the rational design, controllable fabrication and multi-field applications of semiconductor nanostructures, as well as key challenges and interface regulation strategies. Precise preparation of single-unit nanostructures, directional construction of heterostructures, doping modification, and wafer-scale epitaxial growth provide solid support for performance optimization and integration of next-generation devices. Various preparation methods show distinct characteristics and applicable scenarios, requiring rational selection. Benefiting from quantum size, surface and confinement effects, semiconductor nanostructures exhibit excellent performance in optoelectronic, sensing and energy conversion devices. Interface regulation has become the core approach to overcoming fabrication and reliability bottlenecks. Strategies including doping engineering, van der Waals epitaxy, low-temperature etching and heterojunction design effectively improve interfacial quality and carrier transport.

Nevertheless, this review mainly focuses on oxides, perovskites and 2D layered materials, with insufficient discussion on nitrides, carbides and new systems. It also lacks in-depth analysis of industrialization, cost control and AI-assisted design. Future research will prioritize low-cost wafer-scale fabrication and silicon-compatible heterogeneous integration. Multi-field coupling regulation will be explored to realize intelligent and multifunctional devices. Green synthesis systems and stability enhancement via passivation and encapsulation will be developed.The combination with AI and quantum technology will expand applications in quantum computing and communications. Novel low-dimensional nanostructures will continuously break the limits of traditional devices.

In short, semiconductor nanostructures hold great promise for next-generation devices. Driven by continuous technological innovation and interdisciplinary integration, they are expected to achieve broad practical applications and promote the sustainable development of microelectronics and optoelectronics.

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