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Two-dimensional semiconductors for next-generation low-power transistors

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Abstract. As the feature size of silicon-based field-effect transistors approaches its physical limit, the surge in leakage current and static power consumption caused by short-channel effects has become a critical obstacle to sustaining Moore's law. Two-dimensional (2D) semiconductors, with their atomically thin bodies, van der Waals interfaces, and tunable band gaps, offer new material and device strategies to overcome the power bottleneck. Centering on the subthreshold swing—the core figure of merit for low-power transistors—this article reviews the research progress of 2D semiconductors represented by transition metal dichalcogenides, black phosphorus, and tellurene from four dimensions: material systems, device structures, process integration, and application compatibility. It compares the near-ideal switching characteristics of monolayer MoS_2, the high mobility of black phosphorus, and the stability limitations of black phosphorus. It summarizes the roles of gate-all-around architectures, vertical heterojunctions, edge contacts, and wafer-scale integration in improving electrostatic control, reducing contact resistance, and enhancing manufacturability. This article argues that the key challenges for low-power transistors based on 2D semiconductors have shifted from individual performance verification to a comprehensive balance among material stability, contact interfaces, defect control, CMOS compatibility, and scenario-specific reliability.

Keywords: two-dimensional semiconductors, low-power transistors, subthreshold swing, device structure design, contact engineering, wafer-scale integration

1. Introduction

The continuous miniaturization of silicon complementary metal-oxide-semiconductor (CMOS) technology has driven improvements in integrated circuit performance and energy efficiency over the past half-century. However, as transistor channel lengths enter the nanoscale regime, the electrostatic coupling between the source and drain intensifies, and the gate's ability to control the channel potential weakens. The drain-induced barrier lowering (DIBL) effect, together with off-state leakage current, increases rapidly, causing a subsequent rise in static power density and forming a "power wall" that hinders the further extension of Moore's law [1]. The bulk-channel structure of conventional silicon devices still allows leakage paths to form for carriers located far from the gate; therefore, exploring novel channel materials with stronger electrostatic control has become an important research direction for the post-Moore era.

Two-dimensional semiconductors have an atomically thin body thickness, which theoretically allows the gate electric field to fully penetrate the channel, thereby achieving strong control over carrier transport, suppressing short-channel effects, and pushing the subthreshold swing close to the thermodynamic limit of 60 mV/dec at room temperature [1]. This structure eliminates some of the leakage paths inherent in conventional bulk channels and confines carrier transport to an extremely thin region near the gate interface. Since Radisavljevic et al. first reported a monolayer MoS_2 transistor in 2011, related research has expanded from material properties and device structures to process integration and, further, into emerging scenarios such as flexible electronics and neuromorphic computing [2, 3].

This article aims to answer three interrelated questions regarding the practical realization of low-power transistors: which material systems can strike a balance among performance, stability, and manufacturing cost; whether conventional planar device structures need to be modified to accommodate the intrinsic properties of 2D semiconductors; and which types of electronic systems such devices are ultimately suitable for, as well as the requirements that different scenarios impose on their electrical characteristics and reliability. Centered on these questions, this article reviews and comments on twelve representative publications, covering aspects ranging from the theoretical background, material properties, and structural design to process integration and application compatibility.

2. Theoretical background

The switching efficiency of a field-effect transistor from the on-state to the off-state is characterized by the subthreshold swing (SS), defined as the gate-voltage increment required to change the drain current by one order of magnitude, i.e., SS = dVG/d (log10 ID). At room temperature, the thermionic emission mechanism of carriers crossing the source-side potential barrier sets a lower limit for SS of approximately 60 mV/dec. For integrated circuits with continuously decreasing operating voltages, an excessively high SS makes it difficult to fully turn off the device within a limited voltage swing, thereby generating persistent static leakage. Affected by interface trap states, charge sharing, and short-channel effects, the actual SS of conventional silicon transistors often exceeds the theoretical limit. The ultra-thin body of 2D semiconductors can be approximated as an extremely thin electrostatic control layer, enabling the gate voltage to be more effectively converted into a change in the channel surface potential; therefore, it is expected to maintain a high on/off ratio and sufficient on-state current even at operating voltages below 0.5 V [1, 4].

The bandgap is another critical factor determining the off-state leakage current. In logic devices, the bandgap of the channel material must be sufficiently large to suppress thermal excitation and source–drain band-to-band tunneling, yet not so large as to raise the threshold voltage and weaken the low-voltage drive capability. Generally, a moderate bandgap of 1.0–1.5 eV is considered more suitable for low-power devices. Monolayer MoS_2 and other 2D TMDs exhibit a direct bandgap due to quantum confinement effects, with a bandgap of about 1.8–1.9 eV; the bandgap of few-layer black phosphorus can be tuned from 0.3 to 2.0 eV depending on the number of layers [4, 5]. Janus-structured 2D materials, such as MoSSe, can introduce a built-in electric field via asymmetric atomic layers, thereby modulating the bandgap and carrier transport polarity, providing a new degree of freedom for the design of ultra-low-power devices [6].

The contact resistance, Rc, is a major bottleneck limiting the on-state current and transconductance of 2D transistors. The surface of 2D semiconductors is free of dangling bonds, which is beneficial for forming relatively clean van der Waals interfaces but also weakens the orbital hybridization between the metal and the channel, readily leading to a large Schottky barrier. Reducing the contact resistance depends not only on the choice of metal work function but also on the engineering control of interfacial chemical bonding and edge

states [7]. At the same time, the electrostatic integrity of the gate structure determines whether the source–drain leakage paths can be effectively cut off, which is the key reason three-dimensional gate architectures, such as the gate-all-around structure, have been introduced into 2D devices [8]. Furthermore, to move toward integrated circuits, 2D devices must also meet the requirements of CMOS back-end-of-line process compatibility, including low-temperature growth, transfer-free integration, and atomic layer deposition of high-k gate dielectrics [9].

3. Literature review

Since the first report of monolayer MoS_2 transistors in 2011, research on low-power devices based on 2D semiconductors has undergone over a decade of development, forming three major research fronts—material property modulation, device structure innovation, and process integration optimization—and progressively expanding into emerging application areas such as flexible electronics and neuromorphic computing. The following sections provide a review and comparison of representative progress along these dimensions.

3.1. Core material development and property optimization

Materials research for low-power 2D semiconductor transistors has primarily focused on two major systems: transition-metal dichalcogenides (TMDs) and black phosphorus (BP). The studies of these two systems exhibit distinct temporal evolution and complementary performance characteristics.

The landmark work came from Radisavljevic et al. They used mechanically exfoliated monolayer MoS_2 as the channel and HfO_2 as the high-k gate dielectric to fabricate a field-effect transistor with an SS of approximately 74 mV/dec and a current on/off ratio exceeding 10^8 at room temperature, demonstrating for the first time experimentally that 2D TMDs can achieve near-ideal switching characteristics [2]. The performance of this device benefited from the strong coupling of HfO_2 to the channel and the relatively low interface scattering enabled by the dangling-bond-free surface of monolayer MoS_2. This work initiated the study of electronic devices based on 2D semiconductors represented by MoS_2.

Subsequently, Liu et al. systematically investigated how the band gaps of TMDs (including MoS_2, WS_2, $MoSe_2$, etc.) vary with layer number and alloy composition using a combination of first-principles calculations and experiments. They pointed out that the bandgap can be continuously tuned over the range of 1.0–2.0 eV. Still, the lattice disorder introduced by alloying reduces carrier mobility, necessitating a trade-off between bandgap tuning and mobility retention. Their long-term electrical measurements also revealed that the adsorption of water and oxygen at chalcogen vacancies causes threshold-voltage drift and an increase in SS, thereby establishing environmental stability as a critical obstacle to the practical applications of TMDs [4].

In parallel with the development of TMDs, black phosphorus, with its puckered layered structure and anisotropic electrical properties, exhibits high hole mobility and a broadly tunable bandgap. Li et al. noted in their review that black phosphorus transistors have the potential to achieve high on-state current and high on/off ratios at sub-0.5 V operating voltages, making them suitable for ultra-low-power, high-speed devices. However, black phosphorus can oxidize within hours in ambient air, where phosphorus atoms react with oxygen and water to form phosphorus oxides and phosphoric acid, thereby destroying the crystal lattice and introducing charged impurities, which cause a rapid decline in mobility [5]. This chemical instability means that black phosphorus devices must rely on rigorous encapsulation or fabrication in an inert environment.

Beyond TMDs and black phosphorus, two-dimensional tellurene has also attracted attention in recent years. Wang et al. systematically reviewed the synthesis, physical properties, and device applications of tellurene, indicating that it possesses high carrier mobility, relatively good ambient stability, and a tunable

bandgap, making it a potential candidate material for low-power transistors [10]. However, the size and thickness uniformity of tellurene nanosheets grown by current solution-based methods remain limited, and large-area controllable synthesis remains a major challenge.

From a comprehensive view of the material studies, monolayer MoS_2 and black phosphorus each have their own advantages in electrical performance. However, environmental sensitivity not only affects device lifetime but also increases manufacturing costs through additional encapsulation and passivation processes. Emerging materials like tellurene exhibit relatively higher stability, but their fabrication maturity remains insufficient. Therefore, the parallel development of stability enhancement and low-cost passivation schemes is a problem that must be solved for 2D semiconductors to move from performance demonstration to mass production.

3.2. Advanced device structure design and optimization

The development of low-power 2D semiconductor devices shows that relying solely on material optimization is insufficient to exploit their intrinsic advantages fully. At the nanoscale, conventional planar gate structures provide limited electrostatic control over the bottom region of the channel; when the gate-to-channel spacing becomes comparable to the channel length, the bottom leakage paths are difficult to cut off, leading to complete SS degradation. Consequently, device design is gradually shifting from planar gate control to three-dimensional gate-all-around control or vertical transport structures, to achieve more complete channel depletion and stronger leakage suppression.

In this direction, Peng et al. reported a gate-all-around (GAA) transistor based on monolayer MoS_2. Using atomic layer deposition and selective etching, they deposited a gate dielectric and gate metal around a nanowire-like MoS_2 channel, thereby achieving three-dimensional gate wrapping of the channel. Experiments showed that the device can operate in the ultra-low voltage region at a drain voltage of 0.5 V, with an SS close to 70 mV/dec; even when the channel length was scaled down to 10 nm, DIBL remained below 50 mV/V, confirming the strong electrostatic control capability of the GAA architecture in 2D devices [8].

Another structural path is the vertical 2D heterojunction transistor. Zhang et al. vertically stacked p-type and n-type 2D materials to form a tunneling junction or a heterojunction channel, enabling carriers to transport in the vertical direction. The transport distance is controlled by the number of material layers, which is much shorter than the channel length of planar devices. This structure can still achieve steep switching below 0.3 V, and static power consumption can be reduced to the femtowatt-per-micrometer level, providing a structural paradigm for ultra-low-power scenarios such as IoT sensor nodes and implantable medical devices [11].

Das et al., from the perspective of flexible electronics, reviewed the progress in applications of 2D semiconductors, noting that the atomically thin thickness and mechanical flexibility of 2D materials make them suitable for bendable and stretchable devices. Flexible transistors based on TMDs can maintain relatively stable electrical performance under certain bending or tensile strains, offering the possibility for low-power transistor applications in wearable devices [3].

By comparison, the GAA structure focuses on three-dimensional gate control, the vertical heterojunction suppresses short-channel effects by shortening the transport path, and flexible devices exploit the mechanical advantages of 2D materials. These structural innovations illustrate that the low-power potential of 2D semiconductors must be unleashed through structural reconstruction, rather than by simply replicating silicon-based planar structures.

3.3. Key process engineering and integration technology

The performance limits of 2D transistors are ultimately constrained by contact resistance and large-area uniformity in material quality; therefore, process engineering and integration technology serve as the critical

bridge connecting proof-of-concept devices to mass-produced chips. In recent years, research in this direction has centered on key areas such as contact optimization, wafer-scale preparation, and gate dielectric integration, with notable progress in each.

In terms of contact optimization, Wang et al. proposed an edge-contact engineering approach to address excessively high contact resistance in MoS_2 transistors. They exposed the edges of MoS_2 layers via reactive ion etching, leveraging the higher chemical reactivity and stronger orbital hybridization of the edge states to selectively deposit metal on the edges rather than the basal plane, thereby forming low-resistance contacts. Experiments showed that this technique can reduce contact resistance by more than one order of magnitude, thereby significantly improving on-state current and transconductance [7]. However, this process is sensitive to etching conditions: excessive etching can damage the channel, while insufficient etching may fail to expose the edges fully. Its uniformity and general applicability still require verification.

In terms of wafer-scale integration, Akinwande et al. reviewed the progress of metal-organic chemical vapor deposition (MOCVD) and 2D material transfer techniques in the wafer-scale growth of MoS_2 and WS_2 and the preparation of device arrays, demonstrating device uniformity on a 4-inch wafer and low-temperature transfer schemes compatible with silicon-based CMOS back-end-of-line processes [9]. However, the defect density of current wafer-scale 2D materials remains significantly higher than that of mechanically exfoliated single crystals. Chalcogen vacancies, grain boundaries, polymer residues, and mechanical damage can degrade mobility and worsen SS, affecting yield and reliability.

In gate dielectric engineering, the reliable integration of ultrathin high-k gate dielectrics is key to ensuring efficient gate control. The dangling-bond-free surface of 2D semiconductors makes uniform nucleation during atomic layer deposition difficult, leading to island-like growth, pinholes, and charge traps. Chen et al. discussed issues such as charge traps, interface state density, and gate leakage current at the interface between high-k gate dielectrics and the 2D channel, pointing out that van der Waals interface engineering and low-temperature atomic layer deposition can help reduce interface defects and represent important process steps for realizing low-power 2D transistors [12].

From a manufacturing cost perspective, all these processes involve a trade-off between performance and complexity. Edge contacts can improve performance but add etching and selective deposition steps; high-quality gate dielectrics typically require longer atomic layer deposition and annealing processes; wafer-scale integration can amortize the cost per device, but the yield loss caused by material defects has not yet been fully resolved. Therefore, the mass production of low-power 2D transistors requires a synergistic advancement among the simplification of contact processes, the improvement of large-area material quality, and interface optimization.

3.4. Performance comparison of typical 2D semiconductor materials and device structures

To comprehensively compare the performance of different material systems and device structures and to reveal the rationale for technology selection in current research, Table 1 summarizes core performance parameters and engineering characteristics from representative publications.

Table 1. Performance comparison of typical 2D semiconductor materials and device structures

Material Type	Suitable Device Structure	Key Performance Advantages	Major Limitations	References
Monolayer MoS_2(TMDs)	Gate-All-Around(GAA) Architecture	SS close to 70 mV/dec, operation at VDS < 0.5 V, on/off ratio > 10^8, and excellent electrostatic control	High contact resistance frommetal–semiconductor Schottkybarrier; moisture-sensitiveinterlayer van der Waals gaps	[2, 7, 8]
ModifiedTMDs (e.g., alloying)	Optimized Planar Architecture	Continuously tunable bandgap(1.0–2.0 eV), relatively high mobility, and compatibility withstandard photolithography	Insufficient environmental stability, long-term conductance drift, potential mobilitydegradation induced by alloying	[4, 7]
Few-layer blackphosphorus	Vertical 2DHeterojunction Architecture	Hole mobility up to severalhundred $cm^2/V·s$, tunable bandgap (0.3–2.0 eV), and highpotential for ultra-low-voltage operation	Rapid oxidative degradation inair; inert atmosphere required for entire device fabrication; challenging uniformity control	[5, 11]
Tellurene	Flexible and Planar Architectures	High carrier mobility, excellent ambient stability, and tunable bandgap	Large-area controllable synthesis not yet mature; device researchstill in early stages	[10]
Wafer-scale 2D materials(MoS_2/WS_2)	CMOS-compatible hybrid architecture	4-inch wafer-scale uniformity, compatibility with siliconback-end-of-line (BEOL) processes, and suitability for parallel manufacturing	High defect density; mobility andSS degraded relative to exfoliatedsingle crystals; transfer residues compromise reliability	

4. Discussion

Based on the systematic review and comparative analysis of the above literature, it can be concluded that low-power transistors based on 2D semiconductors have advanced from the stage of verifying principle feasibility to the stage of addressing engineering challenges. Through the review of representative publications, this article distills four interrelated scientific and technological challenges currently facing the field.

First, there is a contradiction between material environmental stability and manufacturing cost. The performance degradation of TMDs primarily originates from interlayer water and oxygen intercalation, as well as defect-mediated surface reactions. In contrast, the oxidation of black phosphorus is attributed to direct reactions of phosphorus atoms with oxygen and water [4, 5]. Existing inert-atmosphere encapsulation and atomic-layer-deposition-based passivation schemes are effective in the laboratory but, if applied to large-scale chip production, will significantly increase costs and weaken the competitive advantage over silicon-based devices. Tellurene has relatively good ambient stability, but its synthesis cost and scalability still need optimization [10]. Therefore, low-cost, wafer-level-compatible passivation and encapsulation solutions are a primary task in materials engineering.

Second, the universal control of the Schottky barrier at the metal–2D semiconductor interface. Although edge-contact engineering has achieved relatively good results on MoS_2 [7], black phosphorus is chemically reactive, and conventional etching and metal deposition may cause irreversible damage; the edge states of tellurene also differ from those of MoS_2, so the contact behavior may not be identical. Fundamentally, the interfacial barrier height and Fermi-level pinning depend on the details of metal-induced gap states and chemical bonding, and a unified theoretical model is still lacking. The built-in electric field in Janus 2D materials offers a new avenue for contact modulation, but it remains in the theoretical and preliminary experimental stages [6]. In the future, high-resolution characterization and density functional theory calculations should be combined to establish a database of metal–2D semiconductor contacts.

Third, defect control and CMOS compatibility in wafer-scale integration. Current wafer-scale 2D materials exhibit a relatively high density of defects, such as grain boundaries and vacancies, which act as scattering centers and carrier traps, thereby degrading mobility, SS, and gate-dielectric breakdown characteristics [9]. Simultaneously, the high-temperature growth or annealing of 2D materials conflicts with the thermal budget of CMOS back-end-of-line processes, limiting the feasibility of directly integrating them onto existing silicon chips. The low-temperature, high-quality integration of ultra-thin high-k gate dielectrics is equally critical, because interfacial charge traps can lead to SS degradation and threshold voltage drift [12]. Therefore, low-temperature, high-quality growth, transfer-free in situ integration, and defect-tolerant design rules for 2D devices are the main directions for solving this problem.

Fourth, the differentiated device specification framework is driven by application scenarios. IoT edge sensors require transistors to maintain a high on/off ratio at nanoampere-level currents, imposing extreme requirements on SS and gate leakage current; mobile processors and memories need to provide sufficient drive current below 0.5 V, where the GAA structure has advantages; flexible electronics require devices to maintain stable performance after multiple bending cycles, which places special demands on the mechanical reliability of the materials [3]; aerospace and high-reliability applications focus more on wide-temperature-range stability and radiation hardness. This shows that 2D semiconductor transistors should not pursue a single "universal optimum," but should have their materials, structures, and reliability evaluation standards customized according to the target scenario.

5. Conclusion

Centered on the subthreshold swing, this article systematically reviews research progress on low-power transistors based on 2D semiconductors, exemplified by monolayer MoS_2 and black phosphorus, across four dimensions: materials, structures, processes, and applications.

The atomically thin thickness and strong electrostatic control of 2D semiconductors endow them with the potential to surpass silicon-based transistors in low-power devices. Structural innovations such as gate-all-around architectures and vertical heterojunctions further unleash this potential. The emergence of new 2D materials, such as tellurene and Janus structures, provides new possibilities for diversifying the material system, with tellurene's ambient stability particularly noteworthy.

The core challenges of the current field have shifted from intrinsic performance verification to manufacturability and application compatibility, as manifested in four interrelated problems: the trade-off between material stability and manufacturing cost; universal control of interfacial contacts; wafer-scale defects; CMOS compatibility; and scenario-specific, differentiated design. The quality of the gate dielectric interface and the mechanical reliability in flexible applications constitute new technical dimensions, further enriching the connotation of the challenges.

Future research needs to establish a tighter coupling among fundamental physics, material engineering, and process integration. Oriented by manufacturability, breakthroughs should be sought in areas such as defect-tolerant design, low-temperature integration processes, and application-customized optimization, to propel low-power 2D transistors from proof-of-concept devices toward reliable, low-cost, application-specific chip-level implementations. Emerging fields such as flexible electronics and neuromorphic computing will also provide a broader application space for low-power devices based on 2D semiconductors.

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