

Dominant mechanisms and modulation of grain boundary carrier transport in nanocrystalline semiconductors

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Abstract. The electrical transport properties of nanocrystalline polycrystalline semiconductors often vary with grain size, but this correlation does not prove that size is the sole controlling factor. Grain size reduction is usually accompanied by increased grain boundary density, altering defect occupancy, depletion layer width, and cross-boundary barriers. This paper, based on a grain boundary barrier model, employs literature review and comparative analysis to synthesize experimental results from zero-dimensional quantum dot solids, one-dimensional polycrystalline silicon nanowires, and two-dimensional polycrystalline thin films, analyzing the different effects of geometric scale and grain boundary electrical activity on carrier transport. The results show that average grain size primarily affects the frequency of carrier encounters with the interface and the selectable conductive paths; the energy level, density, occupancy, and atomic structure of grain boundary states determine the degree of obstruction at a single interface and may simultaneously reduce carrier concentration and mobility. Grain boundary orientation, applied bias voltage, and illumination further alter local barriers and recombination behavior. Therefore, material evaluation should combine grain size statistics with local potential, atomic structure, and recombination kinetics, and employ grain boundary engineering techniques such as defect passivation, segregation control, or growth optimization based on the specific system.

Keywords: Nanocrystalline semiconductor, Grain boundary electronic states, Carrier transport, Grain boundary engineering

1. Introduction

Nanocrystalline semiconductors are suitable for low-temperature, large-area fabrication and are widely used in thin-film transistors, sensors, and solar cells. As grain size decreases, the number of grain boundaries per unit volume increases, and conductivity and carrier mobility typically decrease accordingly. However, during annealing, doping, and growth, grain size and grain boundary states often change simultaneously. If only the average grain size is used to determine the transport mechanism, it is difficult to distinguish between the effects of geometric path shortening and grain boundary barrier elevation.

This paper explores under what conditions the electrical properties of grain boundaries are a better explanation of carrier transport than grain size. Using a combination of literature review, theoretical analysis, and case studies, the study compares zero-dimensional quantum dot solids, one-dimensional polycrystalline

silicon nanowires, and two-dimensional polycrystalline thin films, discussing the roles of interparticle coupling, tandem grain boundaries, and in-plane transport networks. Zero-dimensional particle interfaces are not entirely equivalent to traditional grain boundaries; therefore, this paper uses them only as a scale comparison to avoid simply attributing different systems to the same mechanism. This research helps distinguish the different effects of grain size and grain boundary electrical activity on carrier transport and can provide a theoretical reference for grain boundary manipulation and performance optimization in devices such as thin-film transistors, sensors, and solar cells.

2. Theoretical basis of scale and grain boundary transport

2.1. Scale effect in different dimensions

The meaning of scale effect varies with dimension. The diameter of a zero-dimensional quantum dot can change the quantum confinement energy level, but when quantum dots are assembled into a solid, charge carriers still need to pass through ligands and particle surfaces. Zhitomirsky et al. found that enhanced coupling between quantum dots significantly changes transport behavior in solids, indicating that the band gap of a single particle does not represent macroscopic conductivity [1]. The diameter of a one-dimensional nanowire affects the proportion of surface depletion regions; if the wire contains multiple grains, the current must almost pass through each grain boundary one by one, and a few high barriers can control the total resistance. Two-dimensional thin films are not only affected by thickness and shielding ability, but also have in-plane bypass paths, and the current may not pass through all grain boundaries. Therefore, size determines the range of available paths, while dimension determines whether these paths are connected in series or form a network structure.

2.2. Grain boundary electronic states and barrier model

Incomplete coordination, vacancies and impurities at grain boundaries generate localized states in the band gap. Acceptor states become negatively charged after capturing electrons, while donor states become positively charged after losing electrons; the net charge depends on the energy level position, Fermi level and temperature. Charged grain boundaries cause depletion layers and band bending to form in adjacent grains. Seto's model for polycrystalline silicon treats this structure as a double Schottky barrier [2]. When thermal emission is dominant, grain boundaries restrict carrier mobility, as shown in Equation (1).

$$\mu_{GB} \propto \exp\left(-\frac{q\varphi_b}{k_B T}\right) \quad (1)$$

In the formula, μ_{GB} is the grain boundary confinement mobility, φ_b is the barrier height, q is the elementary charge, k_B is the Boltzmann constant, and T is the absolute temperature. The exponential term indicates that a small change in the barrier may also cause a significant difference in mobility. Grain size usually only changes the frequency of grain boundary occurrence, but φ_b directly determines whether charge carriers can cross a certain grain boundary. Yang et al. used 4D-STEM combined with atomic resolution electron microscopy to study SrTiO₃ twin crystals, which directly correlated the grain boundary structure, local composition and electrostatic characteristics [3]. Such results show that grain boundaries of the same area can have different electrical activities.

3. Evidence for grain boundary electrical activity dominating transport

3.1. Limitations of interpretation of average grain size

Average grain size is a statistic; it neither represents the size distribution of grains nor tells us what type of grain boundary the current sample is actually passing through. Assuming two samples have the same average size, one with passivated grain boundaries and the other containing more deep-level traps, the potential barrier and conductivity may still differ significantly despite similar numbers of grain boundaries in the two samples. Conductivity satisfies Equation (2). When grain boundaries trap carriers, the free carrier concentration n decreases; scattering and the potential barrier further reduce the mobility μ . Therefore, grain boundaries may simultaneously affect both parameters in the equation, while grain size itself primarily provides the geometric boundary conditions.

$$\sigma = nq\mu \quad (2)$$

This also explains why the correlation between grain size increase and improved conductivity alone is insufficient. Annealing can both promote grain growth and potentially alter dangling bonds, stress, and impurity distribution. Without measurements of local potential energy or defects, experiments cannot determine whether the performance improvement is due to a reduction in the number of grain boundaries or because individual grain boundaries become more easily passable. A more reliable method of comparison would be to adjust the chemical composition of grain boundaries at similar sizes, or to change the size of grain boundaries under similar conditions.

3.2. Experimental comparison of one-dimensional and two-dimensional systems

Polycrystalline silicon nanowires provide one-dimensional evidence. Amit et al. combined electrical measurements with Kelvin Probe Force Microscopy (KPFM) under applied bias to obtain the local potential difference at different grain boundaries and inverted the energy distribution of the grain boundary states [4]. Shamir et al. further measured the change of the barrier with grain size; under depletion conditions, the barrier height was approximately proportional to the square of the grain radius [5]. This does not mean that size alone determines transport behavior, but rather that size participates in the formation of the barrier through depletion charge. For one-dimensional channels, the insurmountable high barrier limits the performance of the entire nanowire.

The results of the study on two-dimensional monolayer MoS₂ further highlight the importance of grain boundary type. Ly et al. performed four-probe measurements on both sides of a single grain boundary and used Transmission Electron Microscopy (TEM) to determine the orientation difference and atomic structure [6]. The grain-boundary mobility was lowest when the orientation difference was less than 9°; as the incident angle increased, the mobility increased by about two orders of magnitude, reaching about 16 cm²·V⁻¹·s⁻¹ at about 20°. The corresponding barrier decreased from about 0.5 eV at low angles to about 0.15 eV at high angles. The sample was still a monolayer material, and the significant changes were mainly due to the grain boundary structure and barrier, rather than the film thickness. This experiment also reminds us that high-angle grain boundaries are not necessarily worse than low-angle grain boundaries; the judgment must be based on the specific atomic structure.

3.3. Scope of the grain boundary dominance conclusion

Not all nanoscale semiconductors are grain boundary dominant. High doping narrows the depletion layer and enhances tunneling; after sufficient passivation, scattering by phonons, ionized impurities, or intragranular

point defects may become the main confinement factors. In zero-dimensional systems, when strong quantum confinement is achieved, particle size may have a greater impact on the band gap than interface differences. Some two-dimensional grain boundaries can form conductive channels along the interface. Therefore, the conclusions in this paper apply to systems where grain boundaries have significant traps or barriers, charge carriers need to cross the boundaries multiple times, and contact resistance has been eliminated.

4. Grain boundary regulation and characterization

4.1. Defect passivation and local potential regulation

Improving transport performance does not necessarily depend on continuous grain growth. Hydrogen can terminate dangling bonds in silicon, while heteropolymers can change the charge and local band of grain boundaries. However, excessive treatment doses may also generate new defects. Nicoara et al. studied Cu(In,Ga)Se₂ absorber layers treated with KF, RbF and CsF and found that the change in grain boundary surface potential is related to the open-circuit voltage of the device; heavier alkali metals can improve passivation by reducing charged defects and promoting the formation of secondary phases at grain boundaries [7]. This result directly links local changes at grain boundaries to device performance, rather than simply attributing performance improvement to average grain size.

Experiments on perovskite materials also show that only treatment methods that truly penetrate the grain boundaries can effectively reduce grain boundary recombination. Ni et al. measured the average grain boundary recombination rate of polycrystalline halide perovskites to be approximately 2200 to 3300 cm²·s⁻¹. Traditional surface treatments have limited effectiveness because they cannot reach the grain boundaries buried within them [8]. However, after adopting treatment methods that can penetrate the grain boundaries, the average recombination rate decreased by about four times, reaching a minimum of 410 cm²·s⁻¹. Therefore, the key lies in whether the grain boundaries are effectively contacted and passivated, rather than whether the grains themselves grow.

4.2. Joint characterization under operating conditions

Grain boundary barriers are not fixed resistances; applied bias voltages redistribute local potential drops, and illumination alters quasi-Fermi levels and trap occupancy: shallow traps may lower the barrier once filled, while deeper levels may accelerate nonradiative recombination. KPFM is suitable for measuring surface potentials, but results can be affected by probes, the environment, and surface adsorption. 4D-STEM and STEM-EELS can provide information on atomic structure, local electric fields, and chemical valence states, but require thin samples and may be damaged by electron beams. More comprehensive experiments should compare these local characterizations with temperature transport, four-probe measurements, and time-resolved photoluminescence on the same sample. Only when size, barrier, and recombination kinetics correspond can the true limiting step be determined.

5. Conclusion

Analysis reveals that grain size and grain boundary electrical activity in nanocrystalline polycrystalline semiconductors operate at different levels of influence. Size affects interface density, surface depletion ratio, and selectable conduction paths, while the energy level, occupation, and atomic structure of grain boundary states determine local charge and potential barriers, potentially reducing carrier concentration and mobility. One-dimensional nanowires amplify the effects of high-barrier grain boundaries, while two-dimensional

networks provide bypass paths. Zero-dimensional quantum dot solids further demonstrate that particle energy levels and inter-particle coupling cannot be reduced to a single-scale parameter. Existing experiments support incorporating local barriers, orientation differences, and recombination velocities into the evaluation, but this conclusion only applies to systems with significantly electrically active grain boundaries. The design of practical materials should first identify current-limiting grain boundaries, then select passivation, segregation control, or growth optimization, rather than simply pursuing larger average grain sizes.

This paper primarily employs literature review and cross-material case comparisons but has not yet quantitatively distinguished the effects of grain size, grain boundary state density, and barrier height through univariate experiments on the same material system. Future research could combine methods such as KPFM, 4D-STEM, and thermodynamic transport to focus on the changes in grain boundary barriers under temperature, bias voltage, and illumination, and establish a quantitative relationship between grain boundary structure and device performance.

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